CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method for compensating threshold voltage roll-off comprising the steps of:

designing a semiconductor chip or system having a plurality of transistor devices in which the channel length of each transistor device is equal to L_{nom};

setting off-current of each transistor device to I-off_{max} by predetermining that each transistor device has a channel length equal to L_{max} and then implanting into each channel of each transistor such that threshold voltage is equal to Vt_{min};

testing the off-current of each transistor device; and

biasing the back-gate or the body nodes of some transistor devices that have an off-current that does not meet a preselected specification of about I-off_{max} to increase the threshold voltage to about Vt_{min} thereof thereby compensating threshold voltage roll-off within said semiconductor chip or system.

2. The method of Claim 1 wherein L_{nom} is 25 nm.

3. The method of Claim 1 wherein the off-current setting is controlled by varying implant conditions and ion dosage.

4. The method of Claim 3 wherein the implanting is performed at an energy from about 5 to about 30 keV.

5. The method of Claim 3 wherein the ion dosage for a p-type dopant is from about 1E11 to about 1E14 atoms/cm^2.

6. The method of Claim 3 wherein the ion dosage for an n-type dopant is from about 1E11 to about 1E14 atoms/cm^2.

7. The method of Claim 3 wherein the implanting comprises a p-type dopant selected from ions of Group III elements.

8. The method of Claim 3 wherein the implanting comprises an n-type dopant selected from ions of Group V elements.

9. The method of Claim 1 wherein the biasing occurs after manufacturing of the semiconductor chip or system during testing thereof.

10. The method of Claim 1 wherein the biasing occurs at a time after manufacturing of the semiconductor chip or system and after testing thereof.

11. The method of Claim 1 wherein the biasing is achieved by an external DC voltage source.

12. The method of Claim 1 wherein the biasing is achieved by an internal circuit that can deliver a potential to the back-gate or the body node of the second transistor devices.

13. The method of Claim 1 wherein the biasing is achieved by an external clock system that can deliver a potential.